DOCUMENT-IDENTIFIER: US 20020012762 A1

TITLE: DOUBLE-SIDE THERMALLY CONDUCTIVE ADHESIVE TAPE FOR PLASTIC-PACKAGED ELECTRONIC COMPONENTS

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[0034] A double coated film tape is marketed commercially by 3M, St. Paul, Minn., under the tradename "9731." A firm silicone PSA system is coated on the inside of a 0.055-inch (0.14 mm) thick polyester film carrier, with a high performance acrylic adhesive being coated on the outside of the carrier. Such tape is stated to feature the strong holding power of a silicone adhesive to various silicone surfaces, along with the high adhesion of an acrylic adhesive to a variety of surfaces.

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	5	(sheet adj3 carrier) with (polyimide adj3 tape) with (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 18:50
2	BRS	L2	35	(polyester adj3 tape) with (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:13
3	BRS	L3	20	(polyimide adj3 tape) with (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 18:51
4	BRS	L4	24	(polyimide adj3 layer) same (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 18:54
5	BRS	L5	83	(polyimide adj3 layer) and (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:04

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	634	(polyimide adj3 tape) same (adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:13
7	BRS	L7	292	(carrier) same (polyimide adj3 tape)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:25
8	BRS	L8	65	7 same (adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:25
9	BRS	L9	25	(carrier) same (polyester adj3 tape) same adhesive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:27
10	BRS	L10	5	polyimide with tape with carrier with silicone with adhesive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:29

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	72	polyimide with tape with silicone with adhesive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:34
12	BRS	L12	116	polyester with tape with silicone with adhesive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:46
13	BRS	L13	33	12 and (chip or chips or die or dice)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:51
14	BRS	L14	418	polyester same tape same silicone same adhesive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 19:52
15	BRS	L15	15	14 same (chip or chips or die or dice)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 20:02

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	529	(polyester) same (silicone adj3 adhesive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 20:03

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	581	(438/124).CCLS.	USPAT; US-PGPUB	2003/04/01 09:53
2	IS&R	L152	344	(438/112).CCLS.	USPAT; US-PGPUB	2003/04/01 10:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L2	196	(438/677).CCLS.	USPAT; US-PGPUB	2003/04/02 00:30
2	IS&R	L4	433	(438/614).CCLS.	USPAT; US-PGPUB	2003/04/02 00:56
3	IS&R	L5	298	(438/634).CCLS.	USPAT; US-PGPUB	2003/04/02 01:15
4	IS&R	L10	705	(("438/for.371.ccls.")).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/02 01:26
5	IS&R	L11	63	(("438/for.384.ccls.")).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/02 01:34

US-PAT-NO: 5611884

DOCUMENT-IDENTIFIER: US 5611884 A

TITLE: Flip chip silicone pressure sensitive conductive adhesive

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With respect to the embodiment in FIGS. 5(a)-5(c) in particular, our new tacky conductive **adhesive** can be formed into columns, instead of balls or bumps, as depicted in FIG. 5(a). In this embodiment, it is applied between the flip **chip** and substrate as a **tape**, which includes several superimposed layers of materials. Thus, removable layers form top and bottom surfaces of the **tape**. These removable layers can be made of a sheet or film-like material such as paper, polyethylene, polypropylene, polytetrafluoroethylene, poly(vinyl chloride), or **polyester**. Where paper is used as the removable layer, it is typically treated or coated with polypropylene or a **silicone** oil, in order to provide release from the **adhesive** portions of the **tape**.

US-PAT-NO: 6057042

DOCUMENT-IDENTIFIER: US 6057042 A

TITLE: Organopolysiloxane composition for surface treatment and
surface-treated EPDM articles

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The coating film was cross-cut to make 100 1 mm-squares. An **adhesive tape** (prepared by applying a **silicone adhesive** YR3340, produced by Toshiba **Silicone** Co., Ltd., to a **polyester** film to a thickness of 40 .mu.m and allowing the coated film in a thermo-hygrostat for 48 hours) was stuck onto the cross-cut film and peeled off. The number of the squares remaining on the substrate was counted as an indication of adhesive strength.

PAT-NO: JP403276653A

DOCUMENT-IDENTIFIER: JP 03276653 A

TITLE: MANUFACTURE OF TAPE CARRIER

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CONSTITUTION: A device hole A is made in a tape 1. Then, a polyester tape 3 provided with an adhesive layer 2 having a width capable of closing the device hole A is bonded. In addition, a negative-type solvent-soluble resist 4 is coated in a width wider than the device hole A. The resist 4 is dried; after that, the **polyester tape** 3 is stripped off together with the **adhesive** layer 2. Then, a copper thin film 5 is formed by a sputtering operation and an electroplating operation in a bath of sulfuric acid and copper sulfate. Then, an alkali-soluble resist 6 is coated. The resist 6 is dried; after that, a circuit original sheet is placed on the side of the copper thin film 5; both faces are etched; a circuit is formed. The resist 6 on which the circuit has been formed is stripped off by using an alkaline liquid; after that, the solvent-soluble resist 4 is removed by using a solvent. Leads are treated with an electroless Sn plating operation 7; a tape **carrier** is formed.

US-PAT-NO: 5620928

DOCUMENT-IDENTIFIER: US 5620928 A

TITLE: Ultra thin ball grid array using a flex tape or printed wiring board substrate and method

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In accordance with the method being described, integrated circuit die 40 and substrate 42 are detachably supported on temporary support substrate **carrier** 38 such that integrated circuit die 40 is positioned within central opening 60 of substrate 42 and such that the bottom surfaces of die 40 and substrate 42 lie substantially in a common plane. In the embodiment shown in FIG. 2A, die 40 and substrate 42 are attached to substrate **carrier** 38 using a double sided **adhesive** tape material 70. One example of such an **adhesive** material is double sided **polyimide tape**. Although **polyimide tape** is given as one example of how die 40 and substrate 42 may be attached to substrate **carrier** 38, it should be understood that a wide variety of materials may be used. Reworkable adhesives such as thermoplastics, other types of double side **adhesive** tapes, and a wide variety of other attaching materials and mechanisms all fall within the spirit and scope of the described invention.

12. A method according to claim 11 wherein said dielectric flex tape substrate is detachably attached to said **carrier** plate using a double sided **polyimide adhesive tape**.

DOCUMENT-IDENTIFIER: US 20020145207 A1

TITLE: Method and structure for integrated circuit package

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[0047] An integrated circuit package of the present invention may be formed in a number of ways and for use in a number of different applications. One method for producing the present invention is illustrated in FIGS. 9A to 9F. As shown in FIG. 9A, a conventional tape **carrier** 50 having a patterned conductive layer and a dielectric layer having vias is typically mounted beneath a copper support frame 52 prior to processing. Any conventional two layer or three layer **polyimide tape carrier** can be used. A first layer of **adhesive** 54 can be applied to **polyimide tape carrier** 50 (FIG. 9B). Any standard technique of applying the **adhesive** can be used. For example, a standard heat press technique, b stage (application and partial cure), or the like can be used. Before being attached to tape **carrier** 50, transition medium 56 can be precut to a size at least as large as the die that will be used. Transition medium 42 length l.sub.tm and width w.sub.tm should be at least as long and wide as die 58 length l.sub.d and width w.sub.d. (See FIG. 8). As shown in FIG. 9C, transition medium 56 is then mounted onto the first layer of **adhesive** 54. A second layer of **adhesive** 60 is applied to the top surface of the transition medium 56 (FIG. 9D). A die 58 is typically thinned by back lapping, polishing methods, plasma etching, or the like, prior to mounting on the second **adhesive** layer (FIG. 9E). Bonding wires 62 can

be attached to pads
or other features of the die 58 to electrically connect the die to appropriate
locations on tape **carrier** 50. Die 18 can then be encased or encapsulated using
mold cap 64. (FIG. 9F).

US-PAT-NO: 6251707

DOCUMENT-IDENTIFIER: US 6251707 B1

TITLE: Attaching heat sinks directly to flip chips and ceramic chip carriers

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Integrated circuit components are characterized by large numbers of input and output I/O connection terminals. Organic materials have been used extensively in production of such integrated electronic components. Most common components are manufactured by producing a lead frame on a **polyimide tape**, using an **adhesive** (e.g. epoxy or **silicone** adhesives) to connect the back side of a wire bond chip onto the lead frame **tape** and wire bonding to connect the front of the die to the leads of the frame. The adhesives manufactured for connecting chips to polyimide tape are usually filled with thermoconductive particles to increase heat conduction from the chip and thus minimize chip temperature.

Plastic components are usually manufactured by transfer molding to encapsulate the chip, bond wires, and part of the leads with epoxy to form a plastic substrate. Ceramic components are usually manufactured by providing a cavity under a ceramic substrate into which the chip, bond wires are placed and then the **polyimide tape** is adhesively bonded to the ceramic substrate with epoxy or **silicone** adhesives and the chip and cavity is filled with thermoconductive epoxy or **silicone adhesive**. A ceramic bottom substrate may be

bonded over the bottom of the cavity to protect the bottom of the component.